SIDDHARTH INSTITUTE OF ENGINEERING &TECHNOLOGY:: PUTTUR
ELECTRONICS & COMMUNICATON ENGINEERING

DIGITAL IC APPLICATIONS

QUESTION BANK

UNIT –I

CMOS LOGIC AND BIPOLAR LOGIC AND INTERFACING

1) a) Design a 4-input CMOS AND-OR-INVERTER gate. Discuss its operation with logic diagram and functional table. **5M [L6][CO2]**
   b) Describe the operation of CMOS inverter for LOW and HIGH inputs? **5M [L3][CO2]**
2) a) Draw the circuit diagram of basic CMOS gate and explain its operation? **5M [L3][CO2]**
   b) Compare CMOS, TTL and ECL logic families. **5M [L5][CO1]**
3) a) Draw the circuit diagram of a two input LS-TTL NAND gate and explain the functional behavior? **5M [L3][CO1]**
   b) Explain in detail about basic ECL logic circuit. **5M [L2][CO1]**
4) Discuss about low voltage CMOS logic and interfacing. **10M [L4][CO1]**
5) a) Design CMOS transistor circuit for 2-input AND gate. With the help of function table, explain the circuit. **5M [L6][CO2]**
   b) Design a CMOS circuit that has the functional behavior f(Z)=A.(B+C). **5M [L6][CO2]**
6) a) Design a 2-input AND gate CMOS circuit. Explain its operation with help of function table. **5M [L6][CO2]**
   b) Design CMOS Logic circuit for XOR gate and explain with operational table. **5M [L6][CO2]**

7) a) Design a 4-input CMOS AND-OR-INVERTER gate. Draw the logic diagram and functional table. **5M [L6][CO2]**
   b) Compare Different logic families. **5M [L5][CO1]**
8) a) Design a 2-input NAND gate using diode logic and a transistor inverter. Analyze the circuit with the help of transfer characteristics. **5M [L6][CO1]**
   b) Explain the following terms with reference to TTL gate. **5M [L2][CO1]**
      i) D.C noise margin ii) Logic levels
9) a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation. **5M [L3][CO1]**
   b) Explain TTL and CMOS interfacing. **5M [L2][CO1]**
10) a) State CMOS logic levels. **2M [L2][CO1]**
   b) Define Fan-in, Fan-out. **2M [L2][CO1]**
   c) Draw the symbol of NMOS and PMOS transistor. **2M [L2][CO1]**
   d) Define TTL logic levels and noise margin. **2M [L2][CO1]**
   e) Define static and dynamic power dissipation. **2M [L2][CO1]**

UNIT –II

THE VHDL HARDWARE DESCRIPION LANGUAGE

1) a) Explain the various data types supported by VHDL. Give the necessary examples. **5M [L2][CO3]**
   b) Explain about VHDL program structure. **5M [L2][CO3]**
2) a) Explain about functions and procedures with an examples. **5M [L2][CO3]**
   b) Explain about libraries and packages. **5M [L2][CO3]**
3) a) Discuss about behavioral design element with an example. **5M [L4][CO3]**
   b) Design the logic circuit and write a data-flow style VHDL program for the following function.
   F (P) = ∑A,B,C,D (1,5,6,7,9,13) + d(4,15). **5M [L6][CO6]**
4) Draw and explain in detail about VHDL design flow. **10M [L3][CO3]**
5) a) Write about structural design elements with an example. **5M [L2][CO3]**
   b) Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c d) Also draw the relevant logic diagram. **5M [L2][CO6]**
6) Design the logic circuit and write VHDL program for the following functions.
   a) F(X) = ∑A, B, C, D (0, 2, 5, 7, 8, 10, 13, 15) + d (1, 6, 11). **5M [L6][CO6]**
   b) F(Y) = ∏A, B,C,D (1, 4, 5, 7, 9, 11, 12, 13, 15). **5M [L6][CO6]**
7) Design a logic circuit for 4-bit parallel adder and write the VHDL code in structural style by considering full adder as a component. **10M [L6][CO6]**
8) Explain in detail different modeling styles of VHDL with suitable examples. **10M [L2][CO3]**
9) a) What is the importance of time dimension in VHDL and explain. **5M [L2][CO3]**
   b) Explain the behavioral design elements of VHDL. **5M [L2][CO3]**
10) Write Short notes
   a) Syntax of entity declaration. **2M [L2][CO3]**
   b) Process statement in VHDL. **2M [L2][CO3]**
   c) Difference between Signal and Variable. **2M [L2][CO3]**
   d) Difference between Function and Procedure. **2M [L2][CO3]**
   e) IEEE Library. **2M [L1][CO3]**

UNIT –III

COBINATIONAL LOGIC DESIGN

1. a) Design a 4 to 16 decoder with 74×138 IC's. **5M [L6][CO4]**

   b) Write a VHDL program for the above design. **5M [L2][CO6]**

2. a) Design a Full adder with Half adders logic circuit. **5M [L6][CO4]**

   b) Write VHDL code for the above design in structural model. **5M [L2][CO3]**

3. a) Explain the operation of standard IC for 3X8 decoder with necessary truth table and internal architecture. **5M [L2][CO4]**

   b) Write a VHDL code for the above Standard IC **5M [L2][CO6]**

4. a) Discuss about IC 74X148 in detail. **5M [L4][CO4]**

   b) Write a VHDL for the above IC. **5M [L2][CO6]**

5. a) With the help of logic diagram explain 74×157 multiplexer. **5M [L2][CO4]**

   b) Write a VHDL code for the above IC in data flow style. **5M [L2][CO6]**

6. Design the following functions using PAL and PLA.

   a) $F_1 = \Sigma(0,1,2,5,7,11,13,14) + d(4,8,10)$ **5M [L6][CO6]**

   b) $F_2 = \Sigma(0,3,5,6)$ **5M [L6][CO6]**

7. Design a priority encoder that can handle 32 requests. Use 74×148 and required discrete gates. Provide the truth table and explain the operation. **10M [L6][CO4]**

8. a) Write a VHDL code for 4-bit ALU IC 74x181. **5M [L2][CO6]**

   b) Draw the structure of a 4-bit comparator and briefly explain about it. Write a structural VHDL code for it. **5M [L3][CO4]**

9. a) Draw the logic symbol of 74 x 85, 4-bit comparator and write a VHDL code for it. **5M[L3][CO4]**

   b) Design a 16-bit comparator using 74×85 Ics. **5M [L6][CO4]**

10. Design a 8X8 binary multiplier and write VHDL code for the design. **10M [L6][CO4]**

UNIT –IV

SEQUENTIAL MACHINE DESIGN PRACTICES

1. Write a VHDL code for a serial adder using Mealy type FSM. **10M [L2][CO5]**

2. a) Design a 4-bit Johnson Counter and explain its operation. **5M [L6][CO5]**

   b) Write a VHDL code for the above design. **5M [L2][CO6]**

3. Design an 8 bit parallel in and serial out shift register and explain its operation with the help of timing waveforms. **10M [L6][CO5]**

4. Draw the standard IC diagram of 74x194 and explain its operation. Write VHDL code for 74X194. **10M [L3][CO6]**

5. What is the difference between ring counter and Johnson ring counter? Design a self-correcting 4 bit, 4 state ring counter with a single circulating 0 using 74x194. **10M [L6][CO5]**

6. Design an 8 bit parallel in and parallel out shift register and explain its operation with the help of timing waveforms. **10M[L6][CO5]**

7. a) Design a 4-bit Ring Counter and explain its operation. **5M [L6][CO5]**

   b) Write a VHDL code for the above design. **5M [L2][CO6]**

8. Discuss the logic circuits of 74x377 register. Write a VHDL program for the above logic. **10M [L4][CO5]**

9. a) Design a bit LFSR counter using 74x194.List out the sequence assuming that the initial state 111. **5M [L6][CO4]**

   b) Write a VHDL code for the above design. **5M [L2][CO6]**

10 a) Draw the 4 bit parallel in parallel out shift register. **2M [L3][CO5]**

   b) What is LFSR counter? **2M [L2][CO5]**

   c) Draw the logic diagram of IC 74194. **2M [L3][CO5]**

   d) What is ring counter? **2M [L2][CO5]**

   e) What do you mean by self-correcting counter. **2M [L2][CO5]**

UNIT –V
DESIGN ELEMENTS AND SEQUENTIAL LOGIC DESIGN

1. Write a VHDL code for fixed point to floating point conversion. **10M[L2][CO4]**

2. What is a dual priority encoder? Explain. Write VHDL code for the design. **10M[L2][CO4]**

3. Design a 8-bit barrel shifter using three control inputs. Write a VHDL program for the same in data flow style **10M [L6][CO4]**

4. Write a VHDL code for 4 bit comparator circuit. Using this entity write a VHDL code for 16 bit comparator. **10M [L2][CO4]**

5. a) Distinguish between latch and flip flop .Show the logic diagram for both. Explain the operation with the help of function table. **5M [L4][CO5]**

   b) Write a VHDL code for a D-flip flop in behavioral model. **5M [L2][CO6]**

6. a) Design a synchronous 4-bit up counter. **5M [L6][CO5]**

   b) Write a VHDL code for the above design. **5M [L2][CO6]**

7. a) Distinguish between the synchronous and asynchronous counters **5M [L4][CO5]**

   b) What are the impediments to synchronous design? **5M [L2][CO5]**

8. What is PLD's? Explain in detail with help of neat sketches. **10M [L2][CO4]**

9. Design an 8 bit serial in and serial out shift register and write a VHDL code for it. **10M [L6][CO5]**

10. a) Design an 8 bit serial in and parallel out shift register. **5M [L6][CO5]**

    b) Design a decade counter and explain its operation with necessary waveforms. **5M [L6][CO5]**